Claims

[c1] 1.An input circuit for providing separate scan and shift paths for a device utilizing single input latches, said circuit comprising:
a first latch having a single data input port and a single clock input port and an output port;
a second latch having a single data input port and a single clock input port and an output port
a first clock input that enables selection of a scan chain input at said first latch and said second latch;
a second clock input that enables selection a shift chain input at said first latch and said second latch; and
wherein a selection of a scan chain input for passing to said input ports of said latches occurs exclusive of selection of a shift chain input for passing to said input ports, and vice versa, and wherein said single input latches provide functionality of latches that support multiple inputs.

[c2] 2. The input circuit of Claim 1, further comprising:
means for receiving said scan chain and said first clock input; and
means for receiving said shift chain input and said sec-

ond clock input.

[c3] 3. The input circuit of Claim 1, further comprising:
means for receiving a data signal at a port of said latches, wherein said data signal is one of a scan chain input and a shift chain input;
means for accepting the scan chain input into said latches to commence a scan chain operation within said device when a first clock signal is on; and
means for accepting the shift chain input into said latches to commence a shift chain operation within said device when a second, different clock signal is on, wherein only one clock signal is on at a time and both said scan chain operation and said shift chain operation are supported by said single input, scan only latches.

[c4] 4. The system of Claim 3, wherein:
said means for accepting the scan chain input includes a first NAND gate that receives as inputs a first clock signal along with a scan chain input and yields a scan chain NAND output;
said means for accepting the shift chain input includes a second NAND gate that receives as inputs a second clock signal along with a shift chain input and yields a shift chain NAND output, wherein both said first and second NAND gates process inputs at substantially the same times during an input operation; and

a third NAND gate that receives as input said scan chain NAND output and said shift chain NAND output, wherein both outputs are subsequently NANDed to yield a two-tiered NAND result.

[c5] 5.The system of Claim 4, further comprising a non-inverting buffer that temporarily delays the two-tiered NAND result prior to sending said two-tiered NAND result to said latches as their input, wherein said NAND result is delayed until a respective clock input shuts off.

[c6] 6. The system of Claim 1, wherein said second clock input is ANDed with a shift input to yield a shifted second clock input that is utilized as the second clock input for selection of said shift chain input.

[c7] 7. The input circuit of Claim 1, further comprising an OR gate having inputs of said first clock signal and a result of an ANDing of said second clock signal with a shift input, wherein an output of said OR signal is utilized as the clock input of said latches.

[c8] 8. The input circuit of Claim 1, wherein said first clock signal and said second clock signal each provide a select signal for respectively receiving either said scan chain input or said shift chain input into said latches, wherein further, the selected input provides a respective scan

chain or shift chain operation to be propagated through the device.

[c9] 9. The input circuit of Claim 1, wherein said latches are scan only LSSD latches.

[c10] 10. The input circuit of Claim 1, wherein said device is a semiconductor device and said input circuit is fabricated on said semiconductor device.

[c11] 11. The input circuit of Claim 9, wherein said semiconductor device is an eFuse device.

[c12] 12. In a device that includes multiple electrical fuse (effuse) circuits that are serially
connected, a circuit for programming and testing electrical fuses, said circuit comprising:
an input circuit that enables a scan only latch to be utilized to dynamically select from
among a scan chain path and a shift chain path being inputted to said device utilizing a series of input clock signals operating as MUX selects for the scan only latches to select either said scan chain path or said shift chain path for passing through said device;
serially connected eFuse circuitry comprising:
AND logic having two inputs and an output;
a multiplexer (MUX) having a first input, a second input ,

a select input, and a MUX output, wherein said output of said AND logic is coupled to said select input of said MUX;

wherein, said efuse circuit includes a fuse coupled to a switch that is controlled by signals from a fuse latch, a pattern latch, and a program signal source, said pattern latch being programmed with a fuse blow status indicating whether or not said fuse is to be blown during device testing; and

means for connecting components and signals of said eFuse circuit to said MUX and said AND logic, wherein said MUX and said AND logic provide a bypass function that determines when a shifted "1" that is serially passed to each of said effuse circuits should be forwarded to said fuse latch for initiating a blow of said fuse, wherein when a fuse blow status within said pattern latch indicates that said fuse is not to be blown, said MUX forwards said shifted 1 to a next effuse circuit without forwarding said shifted 1 to said fuse latch; and

coupling means for connecting said input circuit to said serially connected eFuse circuit such that both scan chain path and shift chain path are supported within said device utilizing said scan only latches.

[c13] 13. The circuit of Claim 12, wherein:

a first input of said AND logic is coupled to a comple-

ment signal of said fuse blow status;
a second input of said AND logic is coupled to said program signal source;
said first input of said MUX is coupled to said fuse latch;
said second input of said MUX is coupled to a MUX output of a previous MUX;
and said MUX output of said MUX is connected to a second input of a next MUX.

[c14] 14. The circuit of Claim 13, wherein, said effuse circuit is a first effuse circuit and is
serially connected to at least a second effuse circuit whose fuse bl
ow status indicates no blowing of its fuse and a third effuse circuit whose fuse blow status indicates a blowing of its fuse, said circuit comprising:
means for routing said shifted 1 through said fuse latch of said first efuse circuit, bypassing a fuse latch of said second efuse circuit and routing said shifted 1 through a fuse latch of said third effuse circuit, wherein only said first efuse circuit and said second efuse circuit utilizes processing time for routing said shifted 1 through respective fuse latches.

[c15] 15. In a device that includes a single input scan-only latch and a two-tiered NAND gate circuit configuration providing a resulting output to said single input latch,

and a series of clock inputs, a system for reducing surface area required for supporting both scan chain and shift chain operations within the device, said system comprising:
means for receiving the resulting output at the input port of said latch, wherein said resulting output is one of a scan chain input and a shift chain input;
means for accepting the scan chain input into said latch to commence a scan chain operation within said device only when a first clock input is on; and
means for accepting the shift chain input into said latch to commence a shift chain operation within said device only when a second, different clock input is on, wherein only one clock signal is on at a time and both said scan chain operation and said shift chain operation are supported by said single input scan only latch.

[c16] 16. The system of Claim 15, wherein:
said means for accepting the scan chain input includes a first two-input NAND gate that receives as input a first clock signal along with a ScanIN input and yields a scan chain NAND output;
said means for accepting a shift chain input includes a second two-input NAND gate that receives as input a second clock signal along with a shiftIN input and yields a shift chain NAND output, wherein both said first and

second NAND gates process their respective inputs at substantially the same time during an input operation; and

a third NAND gate that receives as input said scan chain NAND output and said shift chain NAND output, wherein both outputs are subsequently NANDed to yield a two-tiered NAND result.

[c17] 17.The system of Claim 16, further comprising a buffer that temporarily delays the two-tiered NAND result prior to sending said two-tiered NAND result to said latch as the input, wherein said NAND result is delayed until a respective clock input shuts off.

[c18] 18. In a device that includes a single input scan-only latch and a two-tiered NAND gate circuit configuration providing a resulting output to said single input latch, and a series of clock inputs, a method for reducing surface area required for supporting both scan chain and shift chain operations within the device, said method comprising:

receiving the resulting output at an input port of said latch, wherein said resulting output is a selected one of a scan chain input and a shift chain input;

accepting the scan chain input into said latch to commence a scan chain operation within said device only when a first clock input is on; and

accepting the shift chain input into said latch to commence a shift chain operation within said device only when a second, different clock input is on, wherein only one clock signal is on at a time and both said scan chain operation and said shift chain operation are supported by said single input, scan only latch.

[c19] 19. The method of Claim 18, further comprising:
NANDing a first clock signal with a scanIN input in a first NANDing operation;
NANDing a second clock signal with a shiftIN input in a second, substantially simultaneous NANDing operation; and
subsequently NANDing a result of said first NANDing operation on said ScanIN input and said second NANDing operation on said shiftIN input to yield a two-tiered NAND result.

[c20] 20.The method of Claim 19, further comprising buffering the two-tiered NAND result prior to sending said two-tiered NAND result to said latch as the inputs, wherein said NAND result is delayed until a respective clock input shuts off.